

001020" 0325T560

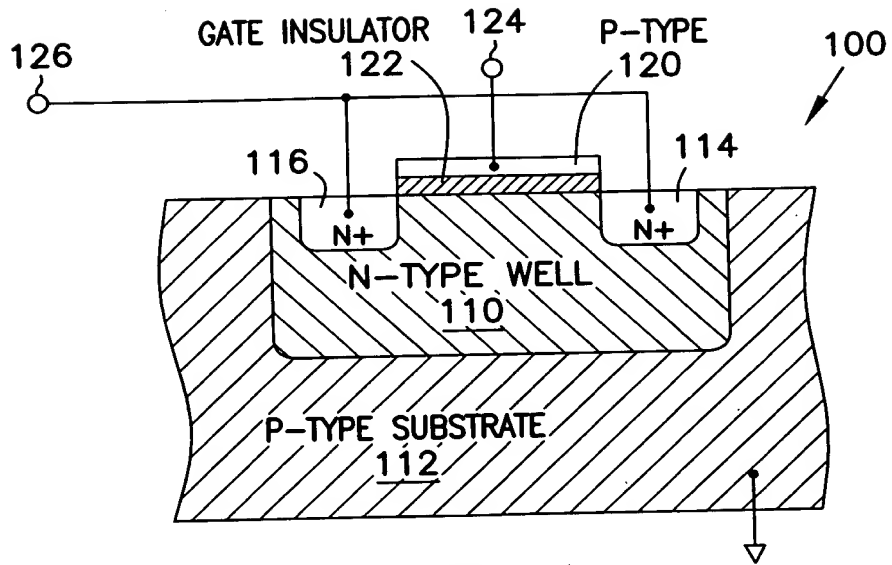


FIG. 1

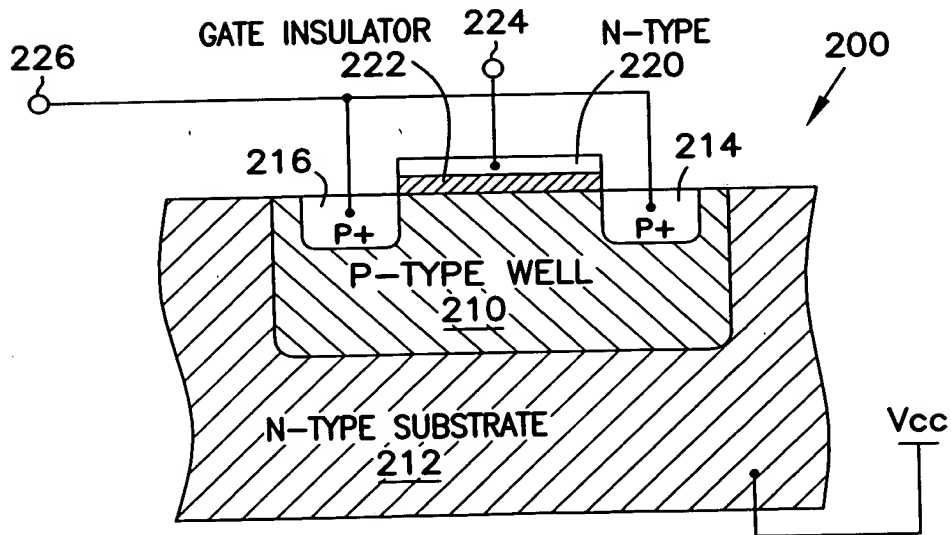


FIG. 2

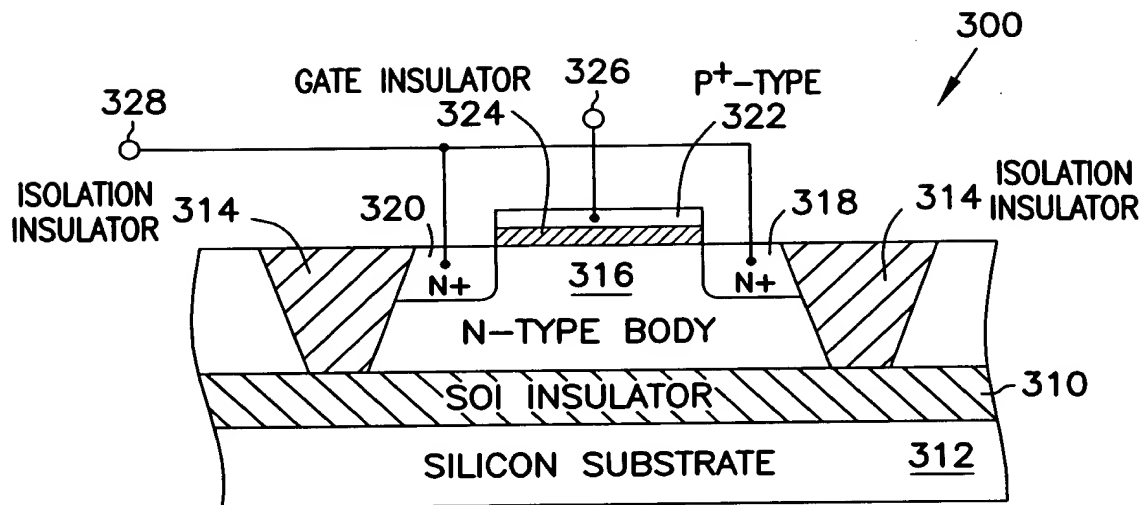


FIG. 3A

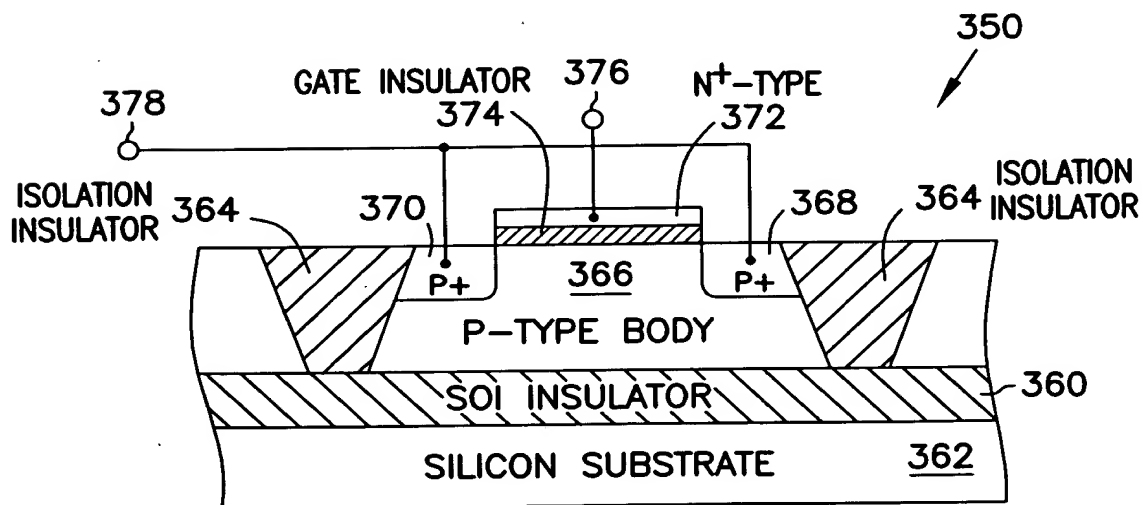


FIG. 3B

A cross-sectional view of a semiconductor device 400. The device is built on a SILICON SUBSTRATE 412, which is covered by a SOI INSULATOR 410. Above the SOI INSULATOR is an N-TYPE BODY 416. The N-TYPE BODY 416 is surrounded by ISOLATION INSULATOR 414. Within the N-TYPE BODY 416, there are two N+ regions 420 and 418. A GATE INSULATOR 424 is positioned over the N-TYPE BODY 416, with a gate electrode 426 on top. The gate electrode 426 is connected to a line 428, which is also connected to the N+ region 420. The N+ region 418 is connected to a line 422, which is also connected to the gate electrode 426. The N+ region 420 is also connected to a line 428, which is also connected to the gate electrode 426.

A cross-sectional view of a semiconductor device 450. The device is built on a silicon substrate 462, which is covered by a silicon oxide insulator (SOI) layer 460. A p-type body 466 is formed in the substrate, with p+ regions 470 and 468. A gate insulator 474 is on top of the body, with a gate electrode 472. A p+ region 476 is also shown. Isolation insulators 464 are on the sides. A contact 478 is connected to the gate electrode.

FIG. 4B

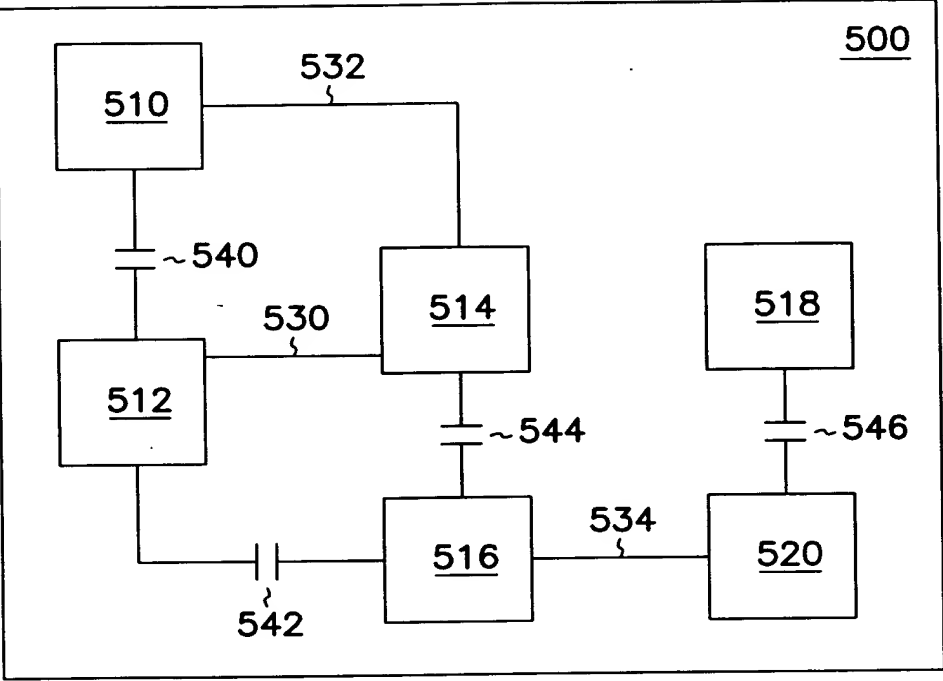
[illegible]

FIG. 5

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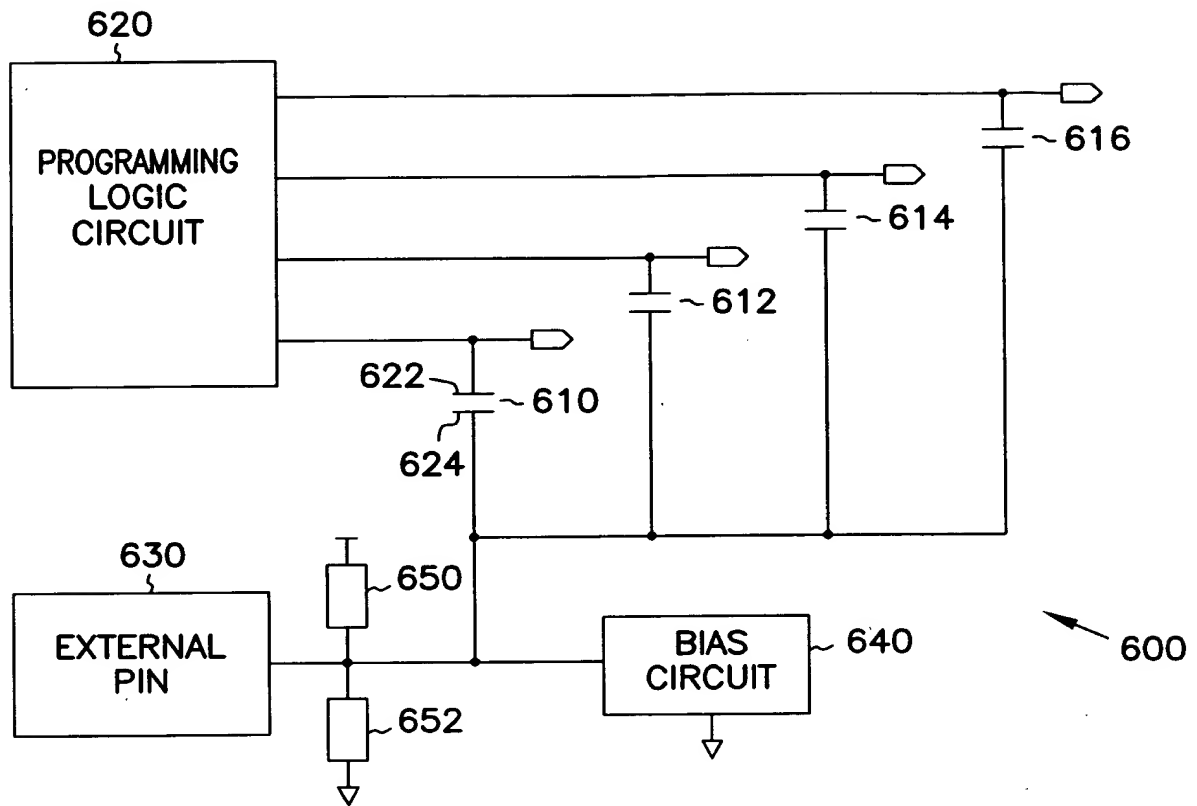


FIG. 6

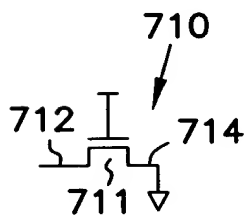


FIG. 7A

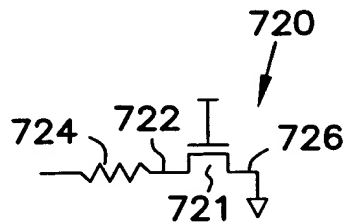


FIG. 7B

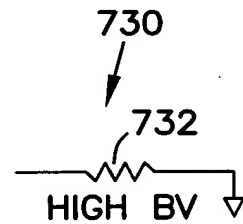


FIG. 7C

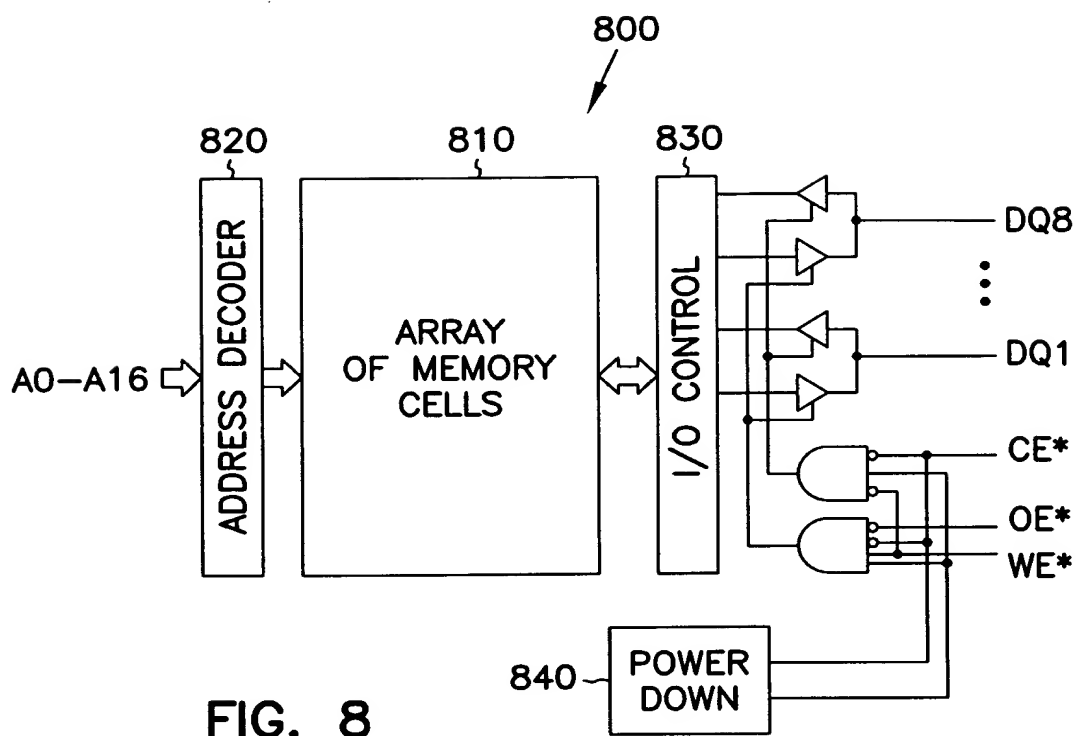


FIG. 8

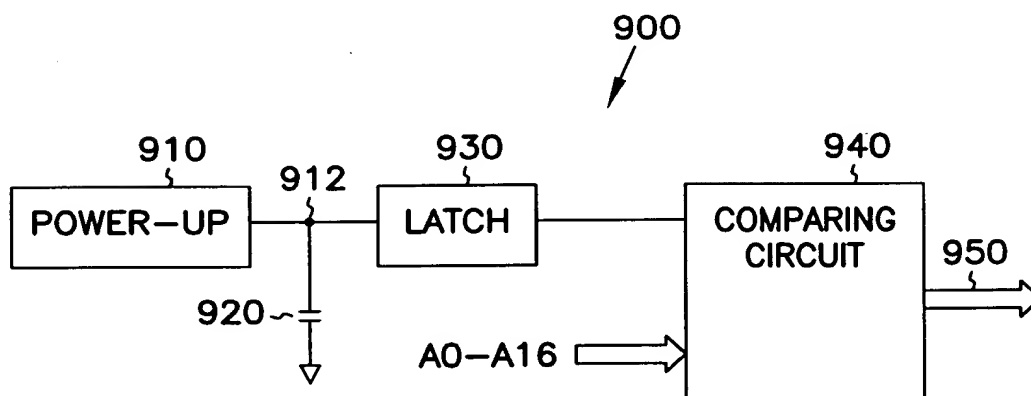


FIG. 9

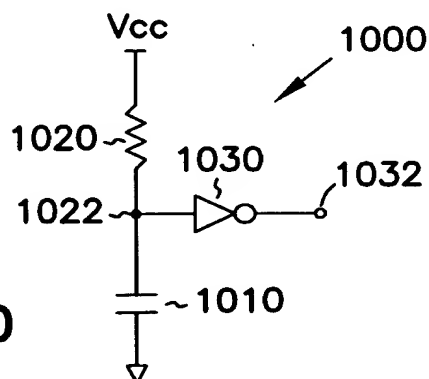


FIG. 10

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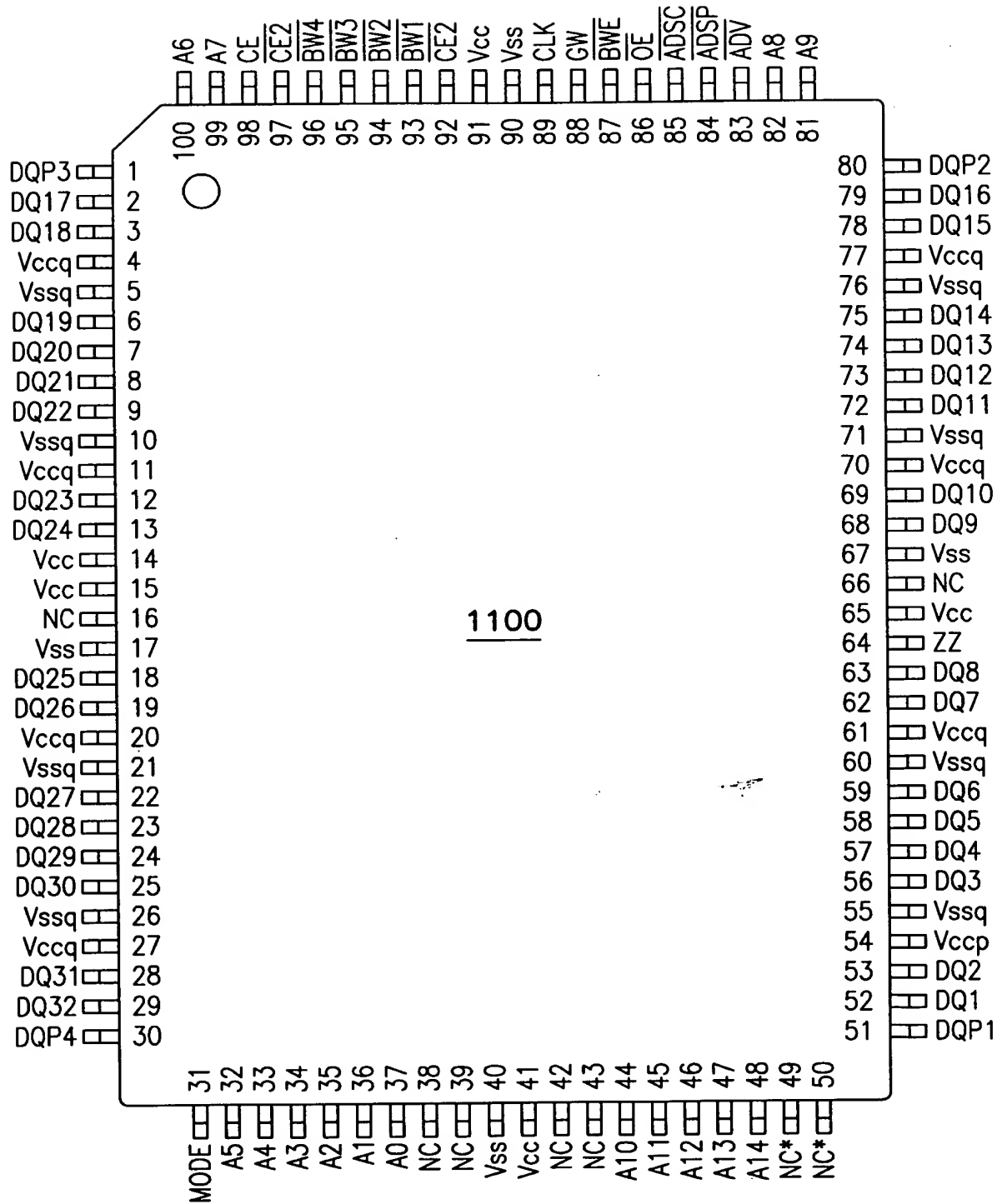


FIG. 11

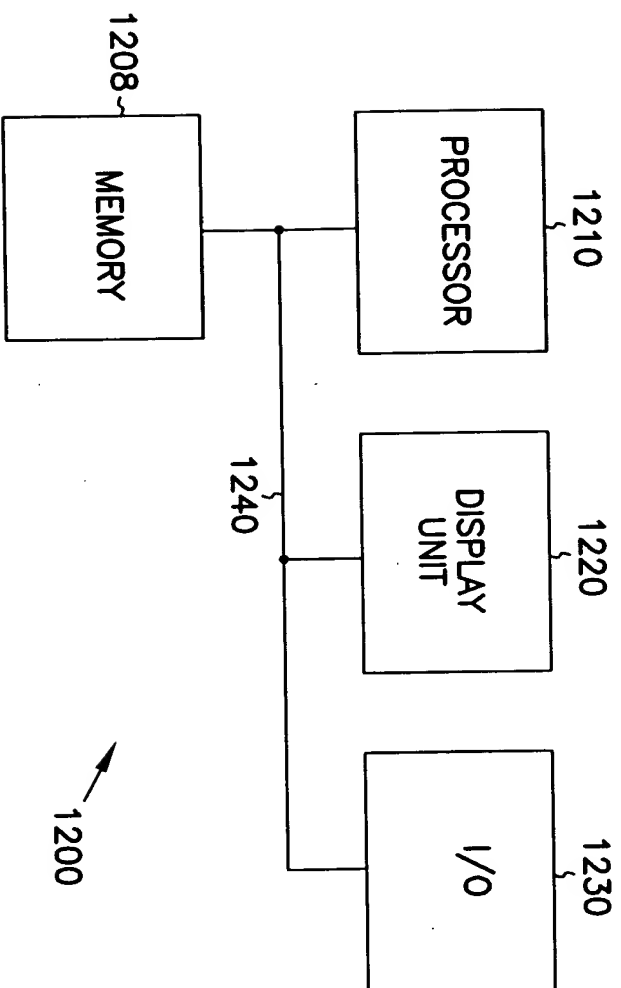


FIG. 12